Amendments to the Specification

Please amend the first paragraph on page 1 as follows:

The whole of the semiconductor industry advancement is centered largely on the development of the device and processing techniques for its Complimentary Metal-Oxide-Semiconductor (CMOS) Field Effect Transistors (FET). In the very early days of MOSFET when aluminum was used as the metal gate, it only appears for a short period of time as the aluminum has a poor adhesion to the Silicon or Silicon di-oxide ($SiO2_2$) and high gate leakage so it was quickly replaced by ~~the~~ poly-silicon with heavily doped N+ dopant. ~~Poly Silicon~~Polysilicon as a metal gate, or in short poly gate, has dominated CMOS technology for more than two decades. It has the advantages of good silicon adhesion, ease of processing, and no metal diffusion or penetration problems. Furthermore, the poly gate electrode can be readily scaled down without major impact to the CMOS processing. In high performance CMOS technology, when the gate size is scaled down to 0.15 and 0.13um, dual doped gate electrodes (~~p~~p+ dopant for the p-channel and n+ dopant for the n-channel) have been used to enhance its channel into surface mode. When CMOS devices are scaled further down to the sub-100nm region, the gate oxide has shrunk to less than 5 nm, and the depletion layer formed in the polysilicon gate in inversion bias becomes a significant fraction of the gate capacitance and degrades the device performance. The use of a metal gate in these CMOS devices can alleviate this problem caused by polysilicon ~~silicon~~ gate associated depletion effects and dopant penetration effects. See "International Technology Roadmap for Semiconductors", Semiconductor Industry Association, San Jose, CA, 2001 (ITRS-2001).

Please amend the first paragraph on page 3 as follows:

US patent 6,511,911 to Besser , et al. gives a metal gate stack structure comprised of Tungsten, tantalum, TiN and etch stopper which is used for the deep submicron CMOS process. Figure 2 depicts the gate stack structure of Besser et al. wherein tungsten is used as capping layer 18 and TiN as the barrier metal 14. ~~There is s~~Second metal layer Ta 16 is deposited in between the capping layer 18 and barrier layer 14.

Please amend the last paragraph on page 4 as follows:

In accordance with the objects of the invention, hafnium nitride (HfN) as the gate material is presented and the formation process of such a gate is given. The semiconductor structure composition consists of at least one underlying dielectric. In common practice, it can be either the conventional SiO_2 or the more recent high dielectric constant (high-K) material of HfO_2, though not only limited to the two. The gate material of HfN exhibits a mid-gap work function and shows robust resistance against high temperature treatment. In particular, the equivalent oxide thickness (EOT) and gate leakage show little variation. The superior oxygen diffusion barrier property as well as the excellent thermal stability of HfN/HfO_2 and HfN/SiO_2 interface makes it an ideal candidate for the sub-65nm for both bulk and SOI CMOS technologies in place of the conventional poly-Si gate material. The gate structure is also ready to be implemented into the symmetrical dual gate transistor structure (SDG).

Please amend the second and third paragraphs on page 5 as follows:

Figure 1 is a cross-sectional representation of a bulk CMOS with metal gate stack structure in the prior art (see US patent 6,225,168 to Gardner et al.) wherein TiN ~~as~~ is the barrier metal ~~22~~ 23 and TaN is the capping layer.

Figure 2 depicts the gate stack structure of the prior art (see US patent 6,511,911to Besser et al.)~~:~~ wherein tungsten is used as capping layer 18 and TiN as the barrier metal 14. ~~There is~~ sSecond metal layer Ta 16 is deposited in between the capping layer 18 and barrier layer 14.

Please amend the last paragraph on page 5 as follows:

Figure 6 through ~~to~~ Figure 10 shows the process steps in forming the bulk CMOS transistor with ~~the said~~ HfN as the metal gate electrode.

Please amend paragraph 3 on page 6 through the paragraph bridging pages 6 and 7 as follows:

A gate dielectric layer 22 is grown or deposited over the substrate to a thickness of between about 15 and 150 Angstroms. For example, the dielectric layer may be a low dielectric constant material such as silicon dioxide, nitrided silicon dioxide, silicon nitride, or their combinations. Alternatively, the dielectric layer may be a high dielectric constant gate dielectric material such as zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxide.

Referring now in particular to Fig. 5, after pre-gate cleaning, the gate dielectric has been thermally grown and the substrate 40 is placed in the PVD vacuum chamber. The PVD chamber is initially set at a base pressure of less than ~~2e-7~~ $2e^{-7}$ Torr~~;~~, flowing the Nitrogen and Argon gases at a constant flow rate of $N2_2$/Ar at ratio of 5 sccm/ 25 sccm, DC power set on the Hf target (42) at 450~~V~~W~~;~~, and RF power set on substrate 40 ~~is set~~ at 12 W. During the sputtering deposition, the gas pressure is maintained at 2 ~~mtorr~~ mTorr inside the chamber. This will lead to a deposition rate of approximately 8.2 nm/min.

A metal layer of HfN 26 (~50 nm) is then formed and the mid gap work function shall be at approximately 4.65eV. This HfN has the composition of Hf/N atomic ratio of 1. To obtain the excellent thermal stability of HfN, the ratio of Hafnium to nitrogen should be controlled to be less than or equal to one (equal amounts or more of nitrogen). By varying the Hf to Nitrogen ratio by way of changing the nitrogen flow, the mid gap work function can be tuned. Alternatively the metal layer 26 may be formed by evaporation, or chemical vapor deposition (CVD). Alternatively, the work function may be tuned or adjusted by impurity doping into the HfN layer.

Please amend the second and third full paragraphs on page 7 as follows:

A TaN (~100 nm) capping layer 28 is sputtered on the HfN gate metal layer to achieve a low gate sheet resistance (~10 Ohm/sq.). The TaN/HfN stack is then etched using a plasma dry etch method (RIE : Reactive Ion Etch) having Chlorine ($Cl2_2$) gas based chemistry. Other capping layers such as tungsten may be used.

Refer now to Figures 6 and 7. The metal and metal capping layers, 26 and 28, respectively, are deposited on the underlying dielectric and then patterned to form gate electrodes. This gate stack contains a first portion 26/28 having the composition of Hafnium and nitrogen and the second portion 22, underlying the first portion, having the composition of Hafnium and oxygen, or silicon and oxygen or other gate dielectric whereas the second portion is in contact with the silicon substrate. A chemical mechanical polishing (CMP) process may be applied to achieve planarization. This gate stack has the capability of scale down to at least below 10Å, and could be utilized ~~at the~~for sub-65nm CMOS technology. The above gate stack structure after thermal treatment of 1000 °C RTA for 20 sec without using surface nitridation prior to HfO_2 deposition, can still maintain very good stability and EOT (equivalent oxide thickness) changes of less than 2 Angstroms.

Please amend the last full paragraph on page 7 as follows:

Referring now to Figures 8 through 10, source and drain regions 30 and sidewall spacers 24 may be formed, as is conventional. The spacers 24 may comprise either silicon nitride or silicon oxide. Processing continues as is conventional in the art.